CLAIMS

1. A trench field effect transistor (trench-FET) comprising:

a semiconductor body having opposed first and second major surfaces;

a source metallisation (22) at the first major surface;

source contact regions (14) of semiconductor doped to have a first conductivity type at the first major surface in contact with the source metallisation (22);

body contact regions (18) of semiconductor doped to have a second conductivity type opposite to the first conductivity type at the first major surface in contact with the source metallisation;

a drain region (2,4) of first conductivity type under the first major surface;

a drain contact (24) connected to the drain region; and

insulated gates (10) including a conductive gate (10) in an insulated trench (6) for controlling current flow between the source contact region (14) and the drain region (2,4) through mesa regions (16) between the insulated gates,

wherein the source contact regions (14) and base contact regions (18) alternate laterally across the first major surface, with the source contact region arranged in the insulated trench (6) above the insulated gate.

2. A trench-FET according to claim 1 wherein the mesa regions comprise doped body regions (20) of semiconductor doped to have the second conductivity type extending under the body contact regions (18) to the drain region (2,4), the doped body regions (20) having a lower doping density than the body contact regions.

3. A trench-FET according to claim 2 wherein the source contact regions (14) extend to a greater depth than the base contact regions (18) so that the source contact regions (14) are in direct contact with the doped body regions (20) under the body contact regions (18) so that current can flow from

the source contact regions (14) through the doped body regions (20) past the insulated gate (10) to the drain regions (2,4).

4. A trench-FET according to claim 2 or 3 wherein the first conductivity type is n-type and the second conductivity type p-type, the p-type doping of the body contact region being above $5x10^{18}$ cm^{-3}, the p-type doping of the body region being in the range 10^{17} cm^{-3} to 10^{18} cm^{-3}, and the doping of the n-type source contact region being above 10^{19} cm^{-3}.

5. A trench-FET according to any preceding claim wherein the drain regions include a drift region (4) of lower doping above a highly doped drain region (2) of higher doping than the drift region, both drain and drift regions being of the first conductivity type.

6. A trench-FET according to claim 5 wherein the doping in the drift region (4) is below 10^{17} cm^{-3} and the doping in the highly doped drain region (2) is above 10^{18} cm^{-3}.

7. A trench-FET according to any preceding claim wherein the source contact regions (14) extend laterally outside the confines of the trenches (6) as well as above the insulated gate (10) so that the width of the body contact regions (22) between the source contact regions (14) is narrower than the width of the mesa regions between the trenches.

8. A method of manufacturing a trench-FET, including the steps of:

providing a semiconductor body (2,4) having opposed first and second major surfaces doped to be of first conductivity type to form a drain region;

implanting a body contact region (18) at the first major surface of semiconductor doped to be of a second conductivity type opposite to the first conductivity type;

forming trenches (6) laterally across the first major surface alternating laterally with the body contact regions (18), the trenches extending below the

body contact regions (18) defining mesa regions below the body contact regions (18) between the trenches (6);

forming insulated gates (10) in the trenches (6);

depositing source regions (14) of semiconductor doped to be of the first conductivity type in the trenches (6) above the insulated gates (10); and

depositing a source metallisation (22) at the first major surface contacting the source regions (14) and the body contact regions (18).

9. A method according to claim 8 further comprising the step of implanting body regions (20) of second conductivity type to a first depth greater than the depth of the source contact regions (14) wherein the body contact implantation (18) is carried out to a second depth less than the first depth.

10. A method according to claim 8 or 9 wherein the step of forming insulating gates (10) in the trenches includes the steps of forming insulator (8,9) on the sidewalls and base of the trenches (6), forming gate conductor (10) in the trenches (6) to a depth below the top of the trenches and forming gate-source insulator (12) in the trenches above the gate conductor (10).